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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,472	09/10/2003	Nadi R. Itani	0876-CS-D1	4320

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EXAMINER	
LAM, HUNG H	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
01/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/659,472	ITANI ET AL.	
	Examiner	Art Unit	
	HUNG H. LAM	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-14 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11 and 38* is/are rejected.

7)☒ Claim(s) *12-14 and 35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the appeal brief filed on 10/21/08, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.
To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 3-11, 14 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Hata (US-6,100,928).

With regarding **claim 3**, Hata discloses a distributed gain control circuit, comprising:

an imager signal source including a shutter (Fig. 1; iris 102 and CCD 103);

a timing circuit for controlling said shutter and the production of signals from said imager signal source (Fig. 1; clock drivers);

a CDS/VGA system (Fig. 2; CDS 104) for receiving imager signals from said imager signal source (CCD 103);

an analog to digital converter (A/D 106) connected to said CDS/VGA system for receiving an amplified imager signal stream from said CDS/VGA system and converting the amplified imager signal stream into digital form (see the connection between A/D 106 and CDS 104);

a digital gain circuit connected to said analog to digital converter (Figs. 1 and 5; IPP 107; Col. 12, Ln. 44-Col. 13, Ln. 3); and

an automatic gain control circuit (Fig. 1; CPU 121; Col. 7, Ln. 4-5) having a gain splitter circuit (CPU 121 splitting control signals to con 1, con 2 and con 3) for receiving gain values which the digital gain circuit have determined (Fig.1 : wherein CPU 121 receives input signal from IPP 107) and wherein the gain splitter circuit (CPU 121) produce distributed gain values from the received gain values (Fig 1: see con 1, con 2 and con 3; Col. 9, Ln. 57-Col. 10, Ln. 65).

With regarding **claim 4**, Hata discloses the DGCC according wherein said AGC circuit (CPU 121) is coupled to said timing circuit (SG 126) for controlling the production of signals from said imager signal source (see Fig. 1; CCD 104).

With regarding **claim 5**, Hata discloses a method of gain control in an imaging system having a shutter (Fig. 1; iris 102 and CCD 103), a digital gain circuit (IPP 107), and a CDS/GA circuit (CDS 104), including:

determining total gain for an imaging system (Fig. 3-4; Col. 10, Ln. 58-Col. 11, Ln. 64; see output from IPP 107 to CPU 121);

receiving, by an automatic, gain control (AGC) circuit having a gain splitter circuit (CPU 121 splitting control signals to con 1, con 2 and con 3), the determined total gain (CPU 121 receive input signals from IPP 107);

splitting, by the gain splitter, circuit, the determined total gain into distributed gain values which at least include a shutter gain (see con 2), and a digital gain (c4); and

determining the level of the shutter gain to be applied in the operation of the imaging system (con 2; see Figs. 3-4; wherein shutter gain is interpreted as shutter speed 1/T);

determining the level of the analog gain to be applied in the operation of the imaging system (see C3); and

determining the level of the digital gain to be applied in the operation of the imaging system (Figs. 1 and 5; IPP 107; Col. 12, Ln. 44-Col. 13, Ln. 3).

With regarding **claim 6**, Hata discloses the method wherein each gain setting for said imaging system is applied for the duration of a single frame (Col. 5, Ln. 35-59; Col. 13, Ln. 1-5).

With regarding **claim 7**, Hata discloses the method including hierarchically adjusting the shutter gain (Fig. 3-4; con 2), the analog (VGA) gain (c3), and the digital gain (c4).

With regarding **claim 8**, Hata discloses the method wherein the shutter gain has maximum and minimum shutter gain values (Fig. 3-4; see maximum and minimum value listed under 1/T).

With regarding **claim 9**, Hata discloses the method wherein the analog (VGA) gain has maximum and minimum analog gain values (AGC 32; Col. 3, Ln. 22-Col. 4, Ln. 20).

With regarding **claim 10**, Hata discloses the method wherein a chip gain has a maximum and a minimum gain value (see Figs. 3-4).

With regarding **claim 11**, Hata discloses the method wherein the digital gain has a maximum and a minimum value (Col. 12, Ln. 44-Col. 13, Ln. 3).

With regarding **claim 38**, Hata the DGCC according to claim 3 wherein the distributed gain values are split into shutter gain values (con 2), analog gain values (c3), and digital gain values (1075; Col. 12, Ln. 60-Col. 13, Ln. 5).

Allowable Subject Matter

4. Claims 12-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 12 the following is a statement of reason for the indication of allowance: the prior art made of record and considered pertinent to the applicant's disclosure does not disclose nor fairly suggest the method of claims 8 further in combination with: **wherein the analog (VGA) gain and the digital gain remain at a constant level as the shutter gain is varied.**

Regarding claim 13 the following is a statement of reason for the indication of allowance: the prior art made of record and considered pertinent to the applicant's disclosure does not disclose nor fairly suggest the method according to claim 8 further in combination with: **wherein the shutter gain and the analog (VGA) gain remain at a constant level as the digital gain is varied.**

Regarding claim 14 the following is a statement of reason for the indication of allowance: the prior art made of record and considered pertinent to the applicant's disclosure does not disclose nor fairly suggest the method according to claim 8 further

in combination with: **wherein the shutter gain and the digital gain remain at a constant level as the analog (VGA) gain is varied.**

Regarding claims 35-37, the claims are being objected as being dependent on the objected claims 12, 13 and 14, respectively.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUNG H. LAM whose telephone number is (571)272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SINH TRAN can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HL
01/21/09

/Sinh N Tran/
Supervisory Patent Examiner, Art Unit 2622